AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A logical simulation system comprising:

delay information operating part which receives a ~~dispersion~~ variation rule file in which information on ~~dispersion in a chip having~~ variation in electrical and physical characteristics ~~which influence~~ influencing the operation of an integrated circuit in a chip ~~to be analyzed~~ is described for each location in the chip, ~~and which receives~~ said delay information operating part further receiving design information of the integrated circuit to prepare a delay information file ~~in consideration of~~ incorporating each influence of said ~~information on said dispersion~~ variation for each location in the chip on the basis of said ~~dispersion~~ variation rule file and said design information; and

logical simulation part which receives said design information and said delay information file to carry out a logical simulation of the integrated circuit.

2. (Currently amended) A logical simulation system as set forth in claim 1, wherein said delay information operating part ~~corrects~~ modifies said design information on the basis of said ~~dispersion~~ variation, and

said delay information file includes the ~~corrected~~ modified design information.

3. (Currently amended) A logical simulation system as set forth in claim 1, ~~which~~ further ~~comprises~~ comprising an information classifying unit which classifies said

information on said ~~dispersion~~ variation into groups of an ~~optional~~ arbitrary size, ~~said groups constituting said chip~~ the chip including said groups, and

wherein said delay information file is prepared so that the influence of said ~~dispersion~~ variation is ~~considered~~ incorporated for every said group.

4. (Currently amended) A logical simulation system as set forth in claim 1, wherein said design information includes actual configuration information which is information on the position of a cell of the integrated circuit in an actual configuration, and

said logical simulation system further comprises a file editing unit which receives said ~~dispersion~~ variation rule file ~~to cause said information on said dispersion to correspond to said actual configuration information to edit said dispersion~~ and edits said variation rule file by incorporating said actual configuration information.

5. (Currently amended) A logical simulation system as set forth in claim 1, wherein said electrical and physical characteristics include ~~a~~ one or more power supply ~~voltage~~ voltages, and

said logical simulation includes ~~verification~~ verifying whether abnormality is caused in the transmission of ~~said~~ a signal ~~by the difference~~ variation in said power supply ~~voltage~~ voltages in the same chip.

6. (Currently amended) A logical simulation system as set forth in claim 2, wherein said electrical and physical characteristics include a power supply voltage, and

said delay information operating unit calculates ~~dispersion~~ variation of signal level caused by ~~dispersion~~ variation in said power supply voltage, and a delay time of signal transmission caused by the ~~dispersion~~ variation of the signal level.

7. (Currently amended) A logical simulation system as set forth in claim 1, wherein said design information includes information on wiring temperature,

said delay information operating unit divides said information on wiring temperature into segments corresponding to said size of said group, and

said delay information file is prepared so that the influence of said ~~dispersion~~ variation is ~~considered~~ incorporated for every said segment.

8. (Currently amended) A computer-executed logical simulation method comprising:

preparing a ~~dispersion~~ variation rule file in which information on ~~dispersion in a chip having~~ variation in electrical and physical characteristics which influence the operation of an integrated circuit ~~being to be analyzed~~ in a chip is described for each location in the chip;

preparing a delay information file ~~in consideration of~~ incorporating each influence of said ~~dispersion~~ variation for each location in the chip on the basis of said ~~dispersion~~ variation rule file and ~~said~~ design information; and

executing a logical simulation of the integrated circuit using said design information and said delay information file.

9. (Currently amended) A computer-executed logical simulation method as set forth in claim 8, ~~which~~ further ~~comprises correcting~~ comprising modifying said design information on the basis of said ~~dispersion~~ variation, and

wherein said delay information file includes the ~~corrected~~ modified design information.

10. (Currently amended) A computer-executed logical simulation method as set forth in claim 8, ~~which~~ further ~~comprises~~ comprising classifying said information on said ~~dispersion~~ variation into groups of an ~~optional~~ arbitrary size, ~~said groups constituting said chip~~ the chip including said groups, and

wherein said delay information file is prepared so that the influence of said ~~dispersion~~ variation is ~~considered~~ incorporated for every said group.

11. (Currently amended) A computer-executed logical simulation method as set forth in claim 8, wherein said design information includes actual configuration information on the position of a cell of the integrated circuit in an actual configuration, and

said computer-executed logical simulation method further ~~comprises causing said information on said dispersion to correspond to said actual configuration information to edit~~ comprising editing said ~~dispersion~~ variation rule file by incorporating said actual configuration information.

12. (Currently amended) A computer-executed logical simulation method as set forth in claim 8, wherein said electrical and physical characteristics include a power supply voltage, and

said executing of ~~said~~ a logical simulation of the integrated circuit includes verifying whether abnormality is caused in the transmission of ~~said~~ a signal by variation ~~by the difference~~ in said power supply voltage in the same chip.

13. (Currently amended) A computer-executed logical simulation method as set forth in claim 8, wherein said electrical and physical characteristics include a power supply voltage, and

said executing of ~~said~~ a logical simulation of the integrated circuit further comprises calculating ~~dispersion~~ variation of signal level caused by ~~dispersion~~ variation in said power supply voltage, and a delay time of signal transmission caused by the ~~dispersion~~ variation of signal level.

14. (Currently amended) A computer-executed logical simulation method as set forth in claim 10, wherein said design information includes information on wiring temperature,

said computer-executed logical simulation method further ~~comprises~~ comprising dividing said information on wiring temperature into segments corresponding to said size of said group, and

said delay information file is prepared so that the influence of said ~~dispersion~~ variation is ~~considered~~ incorporated for every said segment.

15. (Currently amended) A computer-readable recorded medium for use in a computer which receives design information of an integrated circuit to be analyzed to execute a logical simulation of the integrated circuit, said medium having recorded a program for causing said computer to execute a logical simulation method, said method comprising ~~8 comprising~~:

preparing a ~~dispersion~~ variation rule file in which information on ~~dispersion~~ variation in a chip having electrical and physical characteristics which influence the operation of the integrated circuit is described;

preparing a delay information file ~~in consideration of~~ incorporating each influence of said ~~dispersion~~ variation on the basis of said ~~dispersion~~ variation rule file and said design information; and

executing a logical simulation of the integrated circuit using said design information and said delay information file.

16. (Currently amended) A computer readable recorded medium ~~according to~~ as set forth in claim 15, wherein said logical simulation method further comprises ~~correcting~~ modifying said design information on the basis of said ~~dispersion~~ variation, and

said delay information file includes the ~~corrected~~ modified design information.

17. (Currently amended) A computer readable recorded medium ~~according to~~ as set forth in claim 15, wherein said logical simulation method further comprises

classifying said information on said ~~dispersion~~ variation into groups of an ~~optional~~ arbitrary size, ~~said groups constituting said chip~~ the chip including said groups, and

said delay information file is prepared so that the influence of said ~~dispersion~~ variation is ~~considered~~ incorporated for every said group.

18. (Currently amended) A computer readable recorded medium ~~according to~~ as set forth in claim 15, wherein said design information includes actual configuration information on the position of a cell of the integrated circuit in an actual configuration, and

said logical simulation method further comprises ~~causing said information on said dispersion to correspond to said actual configuration information to edit~~ editing said ~~dispersion~~ variation rule file by incorporating said actual configuration information.

19. (Currently amended) A computer readable recorded medium ~~according to~~ as set forth in claim 15, wherein said electrical and physical characteristics include a power supply voltage, and

said executing of ~~said~~ a logical simulation of the integrated circuit includes verifying whether abnormality is caused in the transmission of ~~said~~ a signal ~~by the difference~~ by variation in said power supply voltage in the same chip.

20. (Currently amended) A computer readable recorded medium ~~according to~~ as set forth in claim 16, wherein said electrical and physical characteristics include a power supply voltage, and

said executing ~~of said~~ a logical simulation of the integrated circuit further comprises calculating ~~dispersion~~ variation of signal level caused by ~~dispersion~~ variation in said power supply voltage, and a delay time of signal transmission caused by the ~~dispersion~~ variation of signal level.

21. (Currently amended) A computer readable recorded medium ~~according to~~ as set forth in claim ~~15~~ 17, wherein said design information includes information on wiring temperature,

said logical simulation method further comprises dividing said information on wiring temperature into segments corresponding to said size of said group, and

said delay information file is prepared so that the influence of said ~~dispersion~~ variation is ~~considered~~ incorporated for every said segment.

22. (New) A logical simulation system as set forth in claim 2, wherein said variation in electrical and physical characteristics includes at least one of variation in process, variation in level of power supply voltages for each location in the chip, and variation in junction temperature.

23. (New) A logical simulation system as set forth in claim 2, wherein said electrical and physical characteristics include capacity, and

said delay information operating unit calculates variation of signal level caused by variation in capacities, and a delay time of signal transmission caused by the variation of the signal level.

24. (New) A computer-executed logical simulation method as set forth in claim 8, wherein said variation in electrical and physical characteristics includes at least one of variation in process, variation in level of power supply voltages for each location in the chip, and variation in junction temperature.

25. (New) A computer-executed logical simulation method as set forth in claim 8, wherein said electrical and physical characteristics include capacity; and

said executing a logical simulation of the integrated circuit further comprises calculating variation of signal level caused by variation in capacities, and a delay time of signal transmission caused by the variation of the signal level.

26. (New) A computer readable recorded medium as set forth in claim 15, wherein said variation in electrical and physical characteristics includes at least one of variation in process, variation in level of power supply voltages for each location in the chip, and variation in junction temperature.

27. (New) A computer readable recorded medium as set forth in claim 15, wherein said electrical and physical characteristics include capacity, and

said executing a logical simulation of the integrated circuit further comprises calculating variation of signal level caused by variation in capacities, and a delay time of signal transmission caused by the variation of the signal level.